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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,135	08/17/2001	Steven R. Jahnke	TI-30523	5242

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EXAMINER	
MARTINEZ, DAVID E	
ART UNIT	**PAPER NUMBER**
2182	29

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,135	JAHNKE ET AL.	
	Examiner	Art Unit	
	David E Martinez	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Micro-controller direct memory access (DMA) operation with adjustable word size transfers and address alignment/incrementing".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,297,242 to Miki.

As per claim 1, Miki teaches a data transfer system comprising:

a plurality of bus devices (fig 1, elements 1-5), at least one bus device being a bus data supplying device capable of supplying data (fig 1, elements 3, 4, 5), at least one bus device being a bus data receiving device capable of receiving data (fig 1, elements 3, 4, 5) and at least one bus device being a bus master device capable of requesting and controlling data transfer (fig 1, element 1, column 2, line 65 to column 3, line 10);

a data bus (fig 1, element labeled "System Data Bus (SDB)") connected to each of said plurality of bus devices (fig 1, elements 1-5 see "Branch Data Bus") and capable of transferring data from a bus data supplying device to a bus data receiving device under control of a bus master device (column 2, lines 59-66);

a direct memory access unit (fig 1, element 1) connected to said data bus as a bus master device (fig 1, element 10), said direct memory access unit including

a source word size register storing a source word size (fig 2, element 201, element labeled "PW1", column 3 lines 53-68), and

a target word size register storing a target word size (fig 2, element 202, element labeled "PW2", column 3, lines 53-68),

said direct memory access unit (fig 2, element 1) capable of transferring data from a first bus data supplying device to a first bus data recalling device via said first bus (column

2, lines 59-66) by recalling data from a first bus data supplying device in a data size corresponding to said source word data size and supplying said recalled data to a first bus data receiving device in a data size corresponding to said target word size (see Abstract).

As per claim 2, Miki teaches the data transfer system of claim 1, wherein:

said direct memory access (fig 2, element 1) unit further includes

a read data register loaded with data from said bus data supplying device via said data bus in said source word size (fig 2, element 102, column 3 lines 19-52),

a write data register supplying data to said bus data receiving device via said data bus in said target word size (fig 2, element 112, column 3 lines 19-52), and

a word formatter (fig 2, elements 104, 106, and 108) connected to transfer data from said read data register to said write data register thereby aligning data in said target word size in said write data register (column 3 lines 19-52).

As per claim 3, Miki teaches the data transfer system of claim 2, further comprising:

at least one first bus device being a first bus supplying/receiving device capable of both supplying data to said first bus and receiving data from said first bus (fig 1, elements 1-5).

As per claim 4, Miki teaches the data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit (fig 1, element 2) which is further capable of controlling data transfer (column 3 lines 1-3).

As per claim 5, Miki teaches the data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a direct memory access unit (fig 1, element 1) which is further capable of controlling data transfer (column 2, line 65 to column 3, line 10).

As per claim 6, Miki teaches the data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a memory which is not capable of controlling data transfer (fig 1, element 3).

As per claim 7, the data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit (fig 1, element 2) which is further capable of controlling data transfer (column 3 lines 1-3), said central processing unit connected to said direct memory access unit for loading data into said source data size register and into said target data size register (column 3, lines 53-68).

As per claim 8, the data transfer system of claim 3, wherein:

said direct memory access unit further includes

a source start address register storing a source start address (fig 2, element 201, element labeled "MSTADD1", column 3, lines 53-68),

a source increment size register storing a source increment size (fig 2, element 201, element labeled "BW1", column 3, lines 53-68),

a target start address register storing a target start address (fig 2, element 202, element labeled "MSTADD2", column 3, lines 53-68),

a target increment size register storing a target increment size (fig 2, element 202, element labeled "BW2", column 3, lines 53-68),

said direct memory access unit recalling data from said first bus data supplying device beginning at said source start address and thereafter at successive addresses differing by said source increment size and supplying said recalled data to said first bus data receiving device beginning at said target start address and thereafter at successive addresses differing by said target increment size(column 3, lines 53-68, and abstract).

As per claim 9, Miki teaches the data transfer system of claim 8, wherein:

at least one first bus supplying/receiving device consists of a central processing unit (fig 1, element 2) which is further capable of controlling data transfer (column 3 lines 1-3), said central processing unit connected to said direct memory access unit for loading data into said source start address register, said source increment size register storing, said target start address register and said target increment size register (column 3, lines 53-68, abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10,11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,297,242 to Miki in view of US Patent No. 6,115,767 to Hashimoto et al.

As per claim 10, Miki fails to teach the limitations of claim 10, however Hashitmoto teaches a data transfer system comprising:

a bus arbiter (figs 1, 2, element 9) connected to each of at least one bus master device (fig 1, element 401), a direct memory access unit (figs 1, 2, element 11) and a first bus (figs 1, 2, element 406), the bus arbiter granting control of data transfer on the data bus to one and only one bus master device (column 4, lines 39-50); and

the direct memory access unit further includes

a counter value register storing a number of data words to be transferred by the direct memory access unit (fig 2, element 2, column 5, lines 14-20),

a block size register storing a block size to be transmitted without interruption (fig 2, element 3, column 5, lines 14-20),

the direct memory access unit requesting bus control from a bus arbiter (column 4, lines 39-50) and upon grant of control of data transmission on said data bus, said direct memory access unit thereafter

transferring data in an amount equal to the lesser of said number of data words to be transferred and said block size to be transmitted without interruption, thereafter

ending data transfer if data transferred equals said number of data words to be transmitted, and

suspending data transfer, releasing control of data transfer on said data bus and re-requesting bus control from said bus arbiter (column 5, line 66 to column 6, line 25).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Miki with the teachings of Hashimoto by providing a bus controller, a counter value register, and a block size register such as disclosed Hashimoto, in order to improve overall system performance on the bus, by using DMA transfers that minimize CPU interaction that optimize pipelining of data transfers on the bus.

As per claim 11, the data transfer system, of claim 10, wherein:

at least one first bus supplying/receiving device consists of a central processing unit (fig 1, element 2) which is further capable of controlling data transfer (column 3, lines 1-3), said central processing unit connected to said direct memory access unit for loading data into said counter value register and said block size register.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the central processing unit load data into the counter value register and the block size register since the DMA is controlled by the central processing unit in the first place. As shown by Miki, the central processing unit loads all the necessary values into the DMA that are needed for it to do its data transferring (column 3, lines 53-58)

Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,297,242 to Miki in view of Applicants Admitted Prior Art (AAPA).

As per claim 12, Miki teaches the data transfer system of claim 1, wherein said

plurality of bus devices (fig 1, elements 1-5) consist of first bus devices and said data bus consists of a first data bus (fig 1, element labeled "System Data Bus (SDB)"), said data transfer system (fig 1) further comprising:

a plurality of second bus devices (fig 1, elements 1-5), at least one second bus device being a second bus data supplying device capable of supplying data (fig 1, elements 1, 3, 5), at least one second bus device being a second bus data receiving device capable of receiving data (fig 1, elements 1, 3, 5) and at least one second bus device being a second bus master device capable of requesting and controlling data transfer (fig 1, element 1, column 2, line 65 to column 3, line 10), each second bus device having a predetermined data size (fig 1, data bus shows data width at each device);

Miki teaches all the above limitations except for:

a second data bus having said predetermined data size connected to each of said plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device;

a bus bridge connected to said first data bus and said second data bus, said bus bridge capable of transferring data between said first bus devices and said second bus devices; and

wherein said direct memory access unit stores said predetermined data size in said source word size register for data transfer from a second bus device to a first bus device via said bus bridge and stores said predetermined data size in said target word

size register for data transfer from a first bus device to a second bus device via said bus bridge.

However, AAPA teaches the use of two main busses interconnected by a bridge to separate high performance devices from slower devices so the slower devices do not slow down the access of high performance devices (AAPA, page 2 line 23-29).

AAPA shows high performance devices (fig 1 elements 101, 102, 106, 107, 108) operate on the high performance bus (AHB) (fig 1, element 100), and the slower devices (fig 1, elements 115, 116, 117, 121) operate off of the slower peripheral bus (APB) (fig 1, element 120), and having a bridge (fig 1, element 109), connecting both busses for data transferring and communication.

Miki shows a first bus of predetermined data size, connected to high performance devices and peripheral devices. The DMA module connected to the bus stores a predetermined data size in a source word size register (fig 2, element 201, register labeled "BW1" column 3 lines 53-68) for data transfer from a bus device to another via the bus () and stores a predetermined data size in a target word size register (fig 2, element 202, register labeled "BW2" column 3 lines 53-68) for data transfer from a bus device to another (column 2 lines 59-66). Miki's invention can be modified by adding a second bus for peripheral use thus separating the high performance devices from the slower devices, and having a bridge for data transferring and communication between buses.

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of the AAPA with the teachings of Miki to separate the

high performance devices from the slower performance devices using two different busses interconnected by a bridge for data transferring and communication in order to prevent the high performance devices from being slowed, by the slower peripheral devices.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 6,385,670 to Spilo et al

US Patent No. 4,644,463 to Hotchkin et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E Martinez whose telephone number is (703) 305-4890. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

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